REMARKS

Claims 1-26 are now pending.

The Examiner is thanked for her kind finding of allowable subject matter in claims 21-26. Claims 1, 7, 10, 15, 20-21, and 26 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention, and also to comply with the Examiner's requests set forth in the Office Action. The text of claims 2-6, 8-9, 11-14, 16-19, and 22-25 is unchanged, but their meaning is changed because they depend from amended claims. New dependent claims 27-36 have been added by this amendment and also particularly point out and distinctly claim subject matter regarded as the invention. The amendments are supported by the description on page 12, paragraph **[0018]** of the present specification. No "new matter" has been added by the amendment.

Allowable Subject Matter

The Examiner is thanked for the kind finding of allowable subject matter in claims 21-26 if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph. Applicants acknowledge the Examiner's statement of reasons for allowance as set forth in the Office Action. However, Applicants point out that the reasons for allowability of the above referenced claims are not limited to the reasons for allowance as set forth in the Office Action, and that additional reasons for allowability may exist, each of which may be independently sufficient to establish the patentability of one or more pending claims.

Applicants respectfully reserve the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the claimed invention.

Claim Objections

Claims 7, 20, and 26 stand objected to as allegedly the word "assuming" or "assumes" denotes uncertainty. The claims have been amended to use "setting" or "sets" to eliminate the alleged uncertainty in order to comply with the Examiner's requests set forth in the Office Action. It is respectfully requested that the objection of claims be withdrawn.

The 35 U.S.C. § 112, Second Paragraph Rejection

Claims 1-26 stand rejected under 35 U.S.C. § 112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention. Especially, with respect to claims 1, 10, 15, 20-21, and 26, it is alleged in the Office Action as follows:

> [The claims] recite the limitation of *simulating the global clock net based in part on the simulated load of each of the plurality of clock nets*. However, Applicants' specification at page 14, lines 2-4, precisely states that the simulation is based on the layout, the component values and the simulated clock net loads. Applicants should precisely claim the limitation based on the information in the specification instead of providing the partial recitation.

This rejection is respectfully traversed.

According to M.P.E.P. §2173.02 (Clarity and Precision),

> When the examiner is satisfied that patentable subject matter is disclosed, and it is apparent to the examiner that the claims are directed to such patentable subject matter, he or she should allow claims which define the patentable subject matter with a <u>reasonable</u> degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire.

Also, according to M.P.E.P. §2173.04 (Breadth Is Not Indefiniteness),

> Breadth of a claim is not be equated with indefiniteness. In re Miller, 441 F.2d 689 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intended the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.

Claims 1, 10, 15, 20-21, and 26 has been amended so that they recite "simulating the global clock net based *at least* on the simulated load of each of the plurality of clock nets" (emphasis added) in order to comply with the Examiner's requests set forth in the Office Action. The words "at least" do not exclude other elements on which the simulation may base, and FIG. 6 of the present application discloses the global clock net simulation without particularity of data or parameters on which the simulation bases. The subject matter is the CDM for use with a method/system of determining clock insertion delays, and the claim language particularly recites "the simulated load of the plurality of clock nets," which provides the relationship between the global clock net simulation and the local clock net simulation disclosed in FIG. 6. Thus, the claim language, as amended, define the patentable subject matter with a reasonable degree of particularity and distinctness.

Furthermore, it should be noted the other particular limitations (layout and component values) that the Examiner suggests including are recited in dependent claims 8 and 13. Thus, the claim language of the respective base claims 1 and 10 represents the breadth of the claims, but not imprecision. The scopes of the claims are clear, and there is no indication that the scopes are different from or inconsistent with that defined in the claims.

Accordingly, with this amendment, it is respectfully submitted the claims satisfy the statutory requirements. Withdrawal of the 35 U.S.C. § 112, second paragraph, rejection is respectfully requested.

<u>The 35 U.S.C. § 103 Rejection</u>

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Camporese et al. (U.S. Pat. No. 6,205,571) and Graef (U.S. Pat. No. 6,305,001). This rejection is respectfully traversed.

According to M.P.E.P. § 2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

Claim 1 defines a Clock Data Model (CDM) for use with a method including, among others, simulating each of the plurality of local clock nets to generate a load for

each of the plurality of local clock nets on the global clock net, and simulating the global clock net based at least on the simulated load of each of the plurality of local clock nets. As recited in claim 1, as amended, the plurality of the simulations are stored in the CDM, and especially, the simulated load for each point where the local clock net is connected to the global clock net is stored in the CDM. Claim 15, as amended, also includes the same distinctive features.

Camporese discloses a grid tree clock distribution system which includes a first level tree wiring network **201**, a second level tree wires **203**, and an X-Y grid **204** as shown in FIG. 6 thereof. Camporese also teaches calculating all capacitance loads. However, in Camporese, all capacitance loads are represented at grid intersection points of the X-Y grid-tree (column 7, lines 13-27). As shown in TABLES I and II (columns 7-8), all values of load capacitance are measured at the grid points and represented by a grid capacitance matrix, either before or after the smoothing operation. The key feature of Camporese is to smooth or average the load capacitance value with that of four nearest neighbor grid intersection points, and this operation is done for <u>every</u> element of the grid capacitance matrix (column 8, lines 4-20, emphasis added). Although Camporese uses sector net lists for calculation, the load distribution is still represented by a grid-based point-load capacitance matrix (column 9, lines 35-60, FIGS. 9-10), and there is neither mention to nor suggestion of storing load values at the particular connecting points between the alleged local clock nets (grid tree, or the second clock wires) and the alleged global clock net (H-tree, or the first clock wiring network). Thus, Camporese does not

teach or suggest storing a capacitance load at specific points where a local clock net is connected to the global clock net, as claimed in claims 1 and 15.

Graef teaches planning the clock distribution network, but neither teaches nor suggests storing a capacitance load at points where a local clock net is connected to the global clock net, as claimed.

Accordingly, the claimed invention would not have been obvious from Camporese and Graef, and it is respectfully requested that the rejection of claims based on Camporese and Graef be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-14 and 16-20 depend from claim 1 and claim 15, respectively, and thus include the limitations of claim 1 and claim 15. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reason.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Request for Allowance

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Respectfully submitted,
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Limited Recognition under 37 CFR §10.9(b)

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Version with Markings to Show Changes Made

1. (Twice Amended) A Clock Data Model (CDM) for use with a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning a complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based at least [in part] on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form a complete clock net simulation; and

storing the plurality of simulations in the Clock Data Model, said storing including:

storing the simulated load for each point where the local clock net is connected to the global clock net.

7. (Twice Amended) The CDM as defined in claim 6, wherein said simulating the local clock net includes:

setting clock arrival times from the global clock net to be simultaneous at all points where a given local clock net is connected to the global clock net [are assumed to occur simultaneously when the given local clock net is being simulated].

10. (Twice Amended) The CDM as defined in claim 9, wherein, if the results do not converge, the method further comprises:

setting clock arrival times to be those calculated for the simulated global clock net;

re-simulating the at least one of the plurality of local clock nets using the [a] corresponding calculated clock arrival time, to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based at least [in part] on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net simulation.

15. (Twice Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising means for partitioning a complete clock net into a global clock net and a plurality of local clock nets, means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, means for simulating the global clock net based at least [in part] on the simulated load of each of the plurality of local clock nets, and means for combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

means for storing the plurality of simulation results, said means for storing including:

<u>means for storing the simulated load for each point where the local clock net is connected to the global clock net</u>.

20. (Twice Amended) The CDM as defined in claim 15, wherein the system further comprises means for evaluating the complete clock net to determine whether the results converge, means for <u>setting</u> [assuming that] clock arrival times <u>to be</u> [are] those calculated for the simulated global clock net, means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, means for re-simulating the global clock net based <u>at least</u> [in part] on the simulated or re-simulated load of each of the plurality of local clock nets, and means for combining the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises means for storing the plurality of re-simulation results.

21. (Twice Amended) A Clock Data Model (CDM) for use with a system for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the system comprising a partitioner for horizontally and vertically partitioning a complete clock net into a global clock net and a plurality of local clock nets, at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, a global clock net simulator for simulating the global clock net based <u>at least</u> [in part] on the simulated load of each of the plurality of local clock nets, and a merging unit for

combining the plurality of simulations to form a complete clock net simulation, the CDM comprising:

a memory for storing the plurality of simulation results.

26. (Twice Amended) The CDM as defined in claim 21, wherein the system further comprises a convergence evaluator for evaluating the complete clock net to determine whether the results converge and, when the results are found not to converge, the system <u>sets</u> [assumes that] clock arrival times <u>to be</u> [are] those calculated for the simulated global clock net, the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, the global clock net simulator re-simulates the global clock net based <u>at least</u> [in part] on the simulated or re-simulated load of each of the plurality of local clock nets, and the merging unit combines the simulations and re-simulations to form the complete clock net simulation and wherein the CDM further comprises a memory for storing the plurality of re-simulation results.

27. (New) The CDM as defined in claim 1, wherein said storing the plurality of simulations further includes:

storing clock arrival time and slope for each point where the local clock net is connected to the global clock net.

28. (New) The CDM as defined in claim 27, wherein said storing the plurality of simulations further includes:

storing location of each point where the local clock net is connected to the global clock net.

29. (New) The CDM as defined in claim 1, wherein said storing the plurality of simulations further includes:

storing location of each point where a clocked element is connected to the local clock net.

30. (New) The CDM as defined in claim 29, wherein said storing the plurality of simulations further includes:

storing a name of the clocked element for each point where the clocked element is connected to the local clock net.

31. (New) The CDM as defined in claim 29, wherein said storing the plurality of simulations further includes:

storing clock arrival time and slope of the clocked element for each point where the clocked element is connected to the local clock net.

32. (New) The CDM as defined in claim 15, wherein said means for storing the plurality of simulations further includes:

means for storing clock arrival time and slope for each point where the local clock net is connected to the global clock net.

33. (New) The CDM as defined in claim 32, wherein said means for storing the plurality of simulations further includes:

means for storing location of each point where the local clock net is connected to the global clock net.

34. (New) The CDM as defined in claim 15, wherein said means for storing the plurality of simulations further includes:

means for storing location of each point where a clocked element is connected to the local clock net.

35. (New) The CDM as defined in claim 34, wherein said means for storing the plurality of simulations further includes:

means for storing a name of the clocked element for each point where the clocked element is connected to the local clock net.

36. (New) The CDM as defined in claim 34, wherein said means for storing the plurality of simulations further includes:

means for storing clock arrival time and slope for each point where the clocked element is connected to the local clock net.